Fig. 1

(Prior Art)

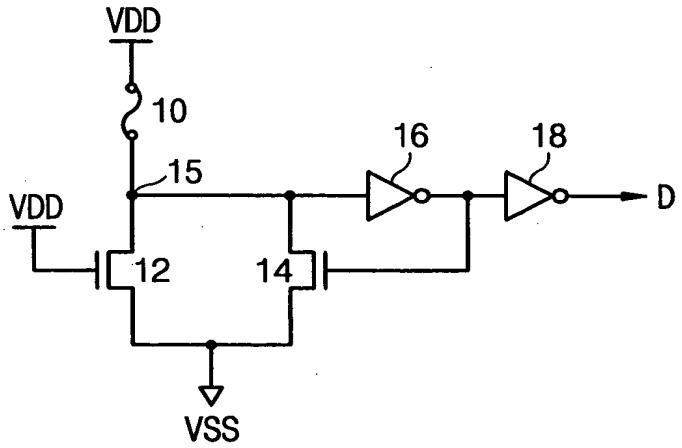


Fig. 2

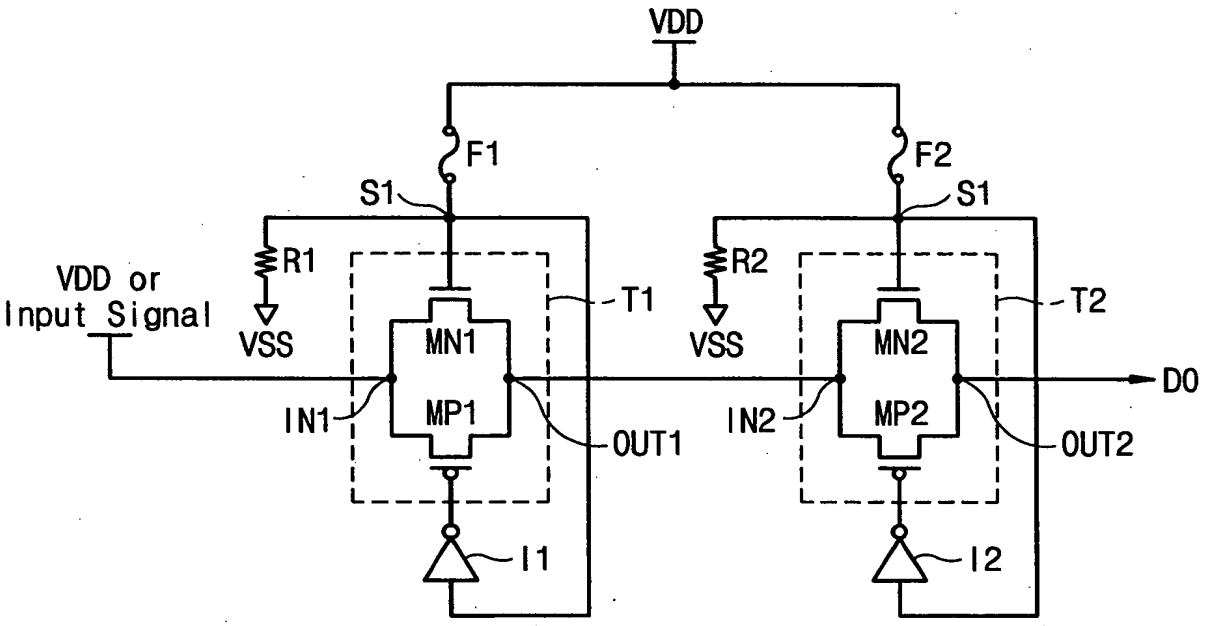
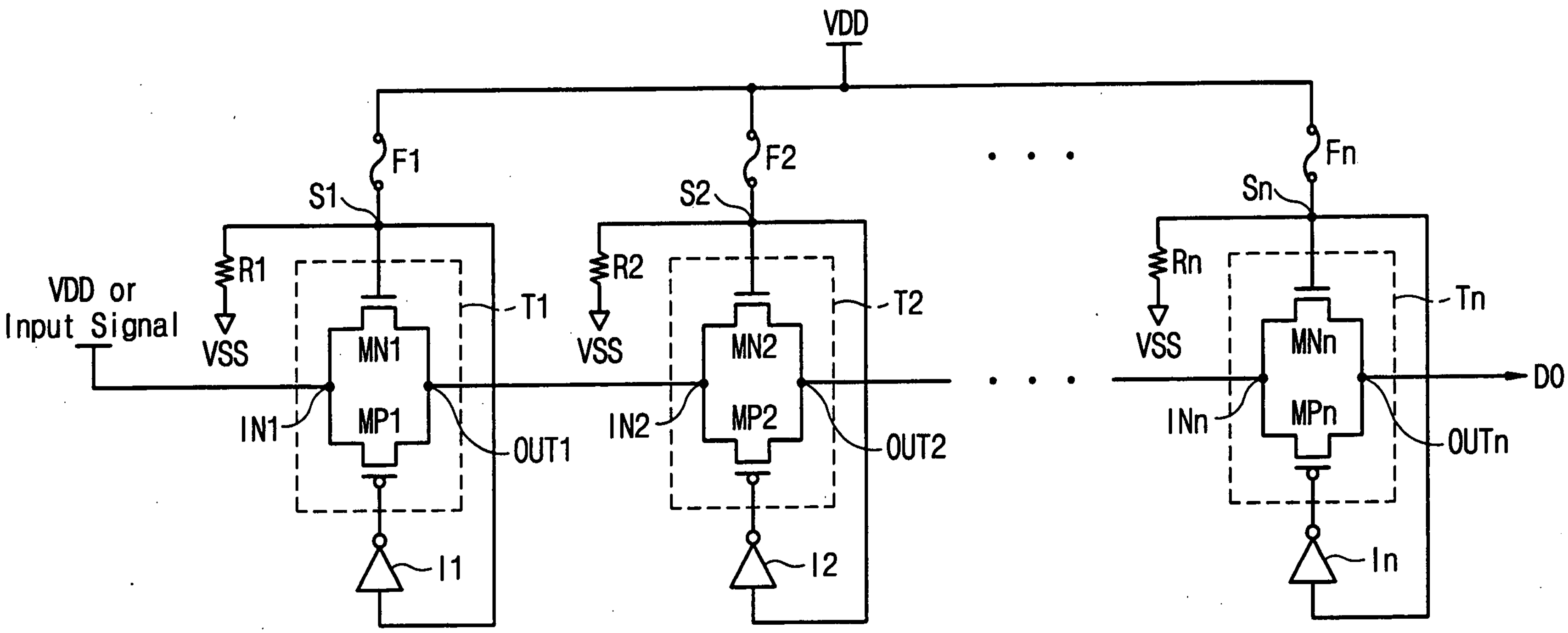


Fig. 3


VDD
F1
F2
Fn
S1
S2
Sn
R1
R2
Rn
VSS
VSS
VSS
VDD or
Input Signal
T1
T2
Tn
MN1
MP1
MN2
MP2
MNn
MPn
IN1
IN2
INn
OUT1
OUT2
OUTn
I1
I2
In
DO